CEYU (ENTROPY) XU

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EDUCATION

Duke University, Durham, NC *August 2020 - Present*
Ph.D. in Computer Science
- Advisor: Prof. Lisa Wu Wills
- Expected Graduation Date: September 2024
- Lab Website: https://apexlab-duke.github.io/

University of California Irvine, Irvine, CA *September 2017 - March 2020*
Bachelor of Science in Computer Engineering
- GPA: 3.847
- Received Magna Cum Laude Latin award

TECHNICAL SKILLS

Compiler:	LLVM, PyTorch Backend, TVM
EDA:	FIRRTL, CIRCT, Yosys, Synopsys and Cadence Toolchains
Computer Architecture:	Transformer Model Hardware Accelerator, Processor Microarchitecture, Machine Learning for Computer Architecture, Cache and Memory-subsystem

PUBLICATIONS

[ISCA 2022] SNS's not a Synthesizer: A Deep-Learning-Based Synthesis Predictor
- **Ceyu Xu**, Chris Kjellqvist, and Lisa Wu Wills. In The 49th Annual International Symposium on Computer Architecture (ISCA 22).
- https://doi.org/10.1145/3470496.3527444
- Design a deep learning model for making fast and accurate predictions of the power, performance, and area of large-scale arbitrary hardware designs.
- Received Honorable Mention of **IEEE Micro Top-picks Honorable Mention 2023**, recognizing exceptional research in the field of computer architecture.

[Micro 2023] Fast, Robust, and Transferable Prediction for Hardware Logic Synthesis (SNS v2)
- **Ceyu Xu**, Pragya Sharma, Tianshu Wang, and Lisa Wu Wills. In 2023 56th IEEE/ACM International Symposium on Microarchitecture (MICRO).
- https://doi.org/10.1145/3613424.3623794
- Extended the original SNS work to enhance transferability and robustness. Proposed a unique circuit transformation-based contrastive pre-training method, which enabled a general-purpose circuit encoder.

[ASPLOS 2022] ProSE: The Architecture and Design of a Protein Discovery Engine
- Eyes Robson*, **Ceyu Xu*** (Co-first author), and Lisa Wu Wills. In Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2022).
- https://doi.org/10.1145/3503222.3507722
- Designed and validated a hardware accelerator based on heterogeneous systolic arrays to speed up large, long-sequence language models, including protein analysis and ChatGPT-like models.
-The accelerator has 1 to 2 orders of magnitude higher higher energy efficiency than NVIDIA GPUs.

[ISPASS 2023] PyTFHE: An End-to-End Compilation and Execution Framework for Fully Homomorphic Encryption Applications
- Jiaao Ma, **Ceyu Xu**, and Lisa Wu Wills. 2022 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).
- https://doi.org/10.1109/ISPASS57527.2023.00012

- Developed the PyTFHE fully homomorphic encryption framework, which provides an end-to-end solution including compilers and distributed backends. This framework supports execution on both CPUs and GPUs, and maintains state-of-the-art performance among other frameworks.
- **ISPASS 2023 Best Paper Award**

[CODES/ISSS 2023] Special Session: Machine Learning for Embedded System Design
- Erika S. Alcorta, Andreas Gerstlauer, Chenhui Deng, Qi Sun, Zhiru Zhang, **Ceyu Xu**, Lisa Wu Wills, Daniela Sánchez Lopera, Wolfgang Ecker, Siddharth Garg, and Jiang Hu. In 2023 International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS '23 Companion).
- https://doi.org/10.1145/3607888.3608962
- Invited Survey paper in which SNS is discussed.

[ICCAD 2023] MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design
-Wenji Fang, Yao Lu, Shang Liu, Qijun Zhang, **Ceyu Xu**, Lisa Wu Wills, Hongce Zhang, and Zhiyao Xie. In 2023 IEEE/ACM International Conference on Computer-Aided Design (ICCAD).
- https://arxiv.org/abs/2311.08441

RESEARCH EXPERIENCES

Ph.D. Research Assistant at Duke *June 2020 - Present*
- Advised by Prof. Lisa Wu Wills.
- Researching hardware agile development, compilers, hardware logic synthesizers, hardware accelerators for machine learning models, and machine learning models for hardware accelerators.

X-MCMC Based 5G MIMO Decoder *June 2020 - June 2021*
- Design and build a MIMO decoder that implements the X-MCMC decoding algorithm for modern 5G wireless communication.
- This research project was completed in Prof. Alvin R. Lebeck's Lab and involved collaboration with Intel Corporation.

Research Assistant at H.E.R.O Lab at UCI *September 2018 - March 2020*
- Design, test, and install an ultra-low power, Bluetooth-based, high precision EEG and ECG signal sensor and a directional antenna for protecting the fetus and pregnant women and maximizing the performance of the transmission at the same time.
- Developed a real-time database system collecting data from multiple clients.

WORK EXPERIENCES

Cloud Service Provider *October 2018 - Present*
- Built a high-performance global transparent proxy called YHJM which expose all the services on the server in LAN to a public IP address. This protocol enables me to host servers in my dorm at a much lower price than buying from AWS or Azure.
- Partner of HoRain Cloud Service Provider at Tianjing China.

Cryptocurrency Miner *May 2017 - September 2022*
- Built a 129-GPUs mining ETH farm alone.
- Managed 20+ mining rigs with extensive use of automation programs for dynamically switching between cryptocurrency bases.
- Earned me one year of college tuition (around $40,000). Profitability outperforms other farms by 10%.

PROJECTS

NOFS: "Not Only For Silicon" Hardware Logic Synthesizer
- A re-implementation of the Yosys Open Synthesis Suite in Rust.
- NOFS extends Yosys with many modern features, including a distributed SAT Solver, in-memory database, and FIRRTL compatibility.

- NOFS also supports TFHE (Fully Homomorphic Encryption over the Torus) as a backend, allowing us to perform arbitrary operations on encrypted circuit inputs.

Toxic: 4-Bit Minimalism Processors

- Developed a series of simplified 4-bit processors called Toxic, with 4-bit register width, 4-bit instruction width, and 8-bit addressing width. Based on a stack machine architecture, despite having only 16 instructions, it can perform basic microcontroller functions with less than 1000 gates.

AWARD

- **IEEE Micro Top-picks Honorable Mention 2023**
- **ISPASS 2023 Best Paper Award**
- Recipient of IEEE Microwave Theory and Techniques Society (MTT-S) Undergraduate Scholarship 2019
- Recipient of Summer Undergraduate Research Program (SURP) Scholarship at UCI for Summer 2019
- Dean's Honor List of UCI, 2019
- Dean's Honor List of UCI, 2018
- Dean's Honor List of UCI, 2017
- National First Prize, 2017 China Adolescents Science & Technology Innovation
- National First Prize, 2016 China Adolescents Science & Technology Innovation